

TEACHING LEARNING EVALUATION PLAN

THEORY COURSE

NAME OF SUBJECT: Hardware Programming

SUBJECT CODE: 21EC504 / 21EC303

SEMESTER AND YEAR: 5th & 3rd Year

SL NO	U nit	Topic / Subtitle	No. of Session Schedu le	No. of Session Held	Ped ago gy	Activity				Learn ing Outc ome
						No. of Ass.	No. of IT	No. Of Quiz	No. of PPT	
1	1	INTEL 8085 and 8086 ARCHITECTURES Introduction to 8085 - 8085 architecture, pin diagram and interrupts and its types. INSTRUCTION SET & ASSEMBLY LANGUAGE PROGRAMMING WITH 8085 Classification of Instruction Set of 8085, sample programmes, method of data transfer modes, memory mapped and I/O mapped data transfer. Introduction to 8086, 8086 architecture-EU, BIU, maximum and minimum modes, pin diagrams & functioning, interrupts. Instruction set & assembly language programming with 8086 Instruction sets, addressing modes, instruction format and sample programs, data transfer .	9	10	BB	1	1	1	0	
2	2	PERIPHERAL INTERFACES Dynamic RAM Interfacing-Interfacing I/O Ports-PIO 8255-Modes of Operation- Interfacing Analog to Digital Data Converters-Stepper Motor Interfacing, Timer- 8253Programmable Interrupt Controller 8259A-DMA Controller 8257-DMA Transfers & Operations-Programmable, DMA Interface 8237.	9	9	BB	1		1	0	
3	3	8051 MICROCONTROLLERS 8051 C programming basics, time delay, I/O programming, Logic operations, Data conversion programs , Accessing code ROM space , ADC,DAC , Interfacing sensors with 8051 and stepper motors. Interfacing with serial communication and timer interrupts	9	7	BB	1	1	1	0	
4	4	INPUT AND OUTPUT I/O Bit addresses for I/O and RAM – I/O programming – I/O bit manipulation programming. TIMER Programming 8051 Timers – Timer 0 and Timer 1 registers – Different modes of Timer – Mode 0 Programming – Mode 1 Programming – Mode 2 Programming - Mode 3 Programming - Counter programming – Different modes of Counter – Mode 0 Programming – Mode 1 Programming - Mode 2 Programming - Mode 3 Programming (simple programs)	9	7	BB & PP T	1		1	0	
5	5	ARM-32 BIT MICROCONTROLLER applications of ARM, Architecture of ARM Cortex, Various Units in the architecture, Debugging support, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence	9	7	BB & PP T	1	0	1	0	

Ass.: Assignment,

IT: Internal Test, ST: Surprise Test

PPT: Power point Presentation.

S. Suresh Kumar

TEACHING LEARNING EVALUATION PLAN

Semester & Year: 5th Sem & III year

S. No	No. of Experiments	Objectives / Learning Outcomes	Duration of Lab
1	10	Objectives: 1. To practice assembly language programming on 8085 & 8086. 2. To practice fundamentals of interfacing/programming various peripheral devices with Microprocessor. Learning Outcomes: 1. Develop assembly language programs for problem solving using software interrupts and various assembler directives. 2. Implement interfacing of various I/O devices to the microprocessor/microcontroller through assembly language programming.	120 Minutes

Sl no.	Name of the Experiment	Briefing / Demonstration	Practical Scheduled	Evaluation	Practical Evaluation Scheme			
					Algorithm	Source Code	Viva	Total
1	Introduction To 8085 Microprocessor	5 minutes	90 minutes	25 minutes	3	5	2	10
2	Addition of two 8 Bit Numbers	5 minutes	90 minutes	25 minutes	3	5	2	10
3	Subtraction of two 8 Bit Numbers	5 minutes	90 minutes	25 minutes	3	5	2	10
4	Addition of two 16 Bit Numbers	5 minutes	90 minutes	25 minutes	3	5	2	10
5	Subtraction two 16 Bit Numbers	5 minutes	90 minutes	25 minutes	3	5	2	10
6	Multiplication of two 8 Bit Numbers	5 minutes	90 minutes	25 minutes	3	5	2	10
7	Ascending Order	5 minutes	90 minutes	25 minutes	3	5	2	10
8	Descending Order	5 minutes	90 minutes	25 minutes	3	5	2	10
9	Factorial of Given Number	5 minutes	90 minutes	25 minutes	3	5	2	10
10	BCD to Binary Code Conversion	5 minutes	90 minutes	25 minutes	3	5	2	10

S. Srinivasan

TEACHING LEARNING EVALUATION PLAN

THEORY COURSE

NAME OF SUBJECT: Basic Electronic Engineering

SUBJECT CODE:23EC101

SEMESTER AND YEAR: I & 1st year

SL .N O	U ni t	Topic /Subtitle	No. of Session Schedule	No. of Session Held	Peda gogy	Activity				Learning Outcome
						No. of Ass.	No. of IT	No. Of Quiz	No. of PPT	
1	01	Basic idea about forward bias, reverse bias and VI characteristics, ideal diode, second and third approximation, surface mount diodes, Zener diode, Testing of diode with multi-meter, half wave rectifier, full wave rectifier, bridge rectifier, RC and LC filters, Design of un-regulated DC power supply, Clipping circuit, Clamping circuit, voltage multiplier circuit, Reading datasheet of semiconductor diode.	9	12	BB & PPT	1	1	1	0	
2	02	BJT operation, BJT voltages and currents, CE, CB and CC characteristics, DC load line and bias point, base bias, emitter feedback bias, collector feedback bias, voltage divider bias, Thermal stability, biasing BJT switching circuits, transistor power dissipation and switching time, Testing of bipolar junction transistor with multi-meter, Reading datasheet of BJT.	9	7	BB & PPT	1		1	0	
3	03	Junction field effect transistors(JFET), Comparison of BJT and FET, JFET characteristics, FET, Biasing in ohmic region and active region, amplification and switching, MOSFETs (D-type and E-type MOSFET), CMOS introduction, E-MOSFET amplifier. MOSFET testing, Reading datasheet for FET and MOSFET.	9	7	BB & PPT	1	1	1	0	
4	04	Introduction, Switching and Logic Levels, Digital Waveform. Number Systems: Decimal Number System, Binary Number System, Converting Decimal to Binary, Hexadecimal Number System: Converting Binary to Hexadecimal, Hexadecimal to Binary, Converting Hexadecimal to Decimal, Converting Decimal to Hexadecimal, Octal Numbers: Binary to Octal Conversion. Complement of Binary Numbers. Boolean Algebra Theorems, De Morgan's theorem. Digital Circuits: Logic gates, NOT Gate, AND Gate, OR Gate, XOR Gate, NAND Gate, NOR Gate, X-NOR Gate. Algebraic Simplification, NAND and NOR Implementation: NAND Implementation, NOR Implementation. Half adder, Full adder.	9	9	BB & PPT	1		1	0	
5	05	Light emitting diode (LED), Photo diode, PIN diode, Varactor, Schottky diode, Tunnel diode. The Ideal Op Amp, Inverting and Non – Inverting configurations, Equivalent Circuit model, Op amp application in Integration, Differentiation and Summing Circuits.	9	7	BB & PPT	0	0	1	0	

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S. Srinivasan

TEACHING LEARNING EVALUATION PLAN

THEORY COURSE

NAME OF SUBJECT: Wireless Communication

SUBJECT CODE: 20EE0445/19EC0403

SEMESTER AND YEAR: 7th & 4th Year

SL. NO	Unit	Topic / Subtitle	No. of Session Schedule	No. of Session Held	Pedagogy	Activity				Learning Outcome
						No. of Ass.	No. of IT	No. Of Quiz	No. of PPT	
1	01	CELLULAR CONCEPT Introduction - Standards: Evolution of mobile radio communication fundamentals General Model of Wireless Communication Link, Types of Signals, Cellular Infrastructure, Cellular System Components, Antennas for Cellular Systems, Operation of Cellular Systems, Channel Assignment, Frequency reuse, Channel Assignment strategies, Handoff Strategies Cellular Interferences, Sectorization	9	10	BB	1	1	1	0	
2	02	MOBILE RADIO PROPAGATION Wireless Channel and Radio Communication, Free Space Propagation Model, Channel Noise and Losses, Fading in Land Mobile Systems, Multipath Fading, Fading Effects on Signal and Frequency, Shadowing; Wireless Channel Modeling: AWGN Channel, Rayleigh Channel, Rician Fading Channel, Nakagami Fading Channel, Okumura and Hata Path Loss Model; Channel Modelling: Stochastic, Flat Fading, Wideband Time- Dispersive Channel Modelling.	9	9	BB	1		1	0	
3	03	MODULATION AND SIGNAL PROCESSING Digital modulation techniques for mobile communications: BPSK, DPSK, $\pi/4$ QPSK, OQPSK GMSK, Zero Inter Symbol Interference Communication Techniques, Detection Strategies, Diversity Combining Techniques: Selection Combining, Threshold Combining, Equal Gain Combining, Maximum Ratio Combining; Spatial Diversity and Multiplexing in MIMO Systems, Channel Estimation	9	7	BB	1	1	1	0	
4	04	EQUALIZATION TECHNIQUES Transversal Filters, Adaptive Equalizers, Zero Forcing Equalizers, Decision Feedback Equalizers, and related algorithms; Multiplexing and Multiple Access: FDMA, TDMA, CDMA, OFDMA, SC- FDMA, IDMA Schemes and Hybrid Method of Multiple Access Schemes, RAKE Receiver.	9	7	BB & PPT	1		1	0	
5	05	WIRELESS LAN STANDARD & BLUETOOTH IEEE 802.11 Architecture and Services - IEEE 802.11 Medium Access Control- IEEE 802.11 Physical layer Bluetooth: Overview- Radio specifications-Base band specifications-Link Manager Specification-Logical Link Control and Adaptation Protocol.	9	7	BB & PPT	1	0	1	0	

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S. Sureshankar