CURRICULUM & SYLLABUS

CHOICE BASED CREDIT SYSTEM (CBCS)

FOR

MASTER OF TECHNOLOGY (M.Tech.)

(2 Year Postgraduate Degree Programme)

IN

MICROELECTRONICS

[w. e. f. 2024-2025]

FACULTY OF ENGINEERING AND TECHNOLOGY

SRM UNIVERSITY DELHI-NCR, SONEPAT

39, Rajiv Gandhi Education City, Sonepat

Haryana-131029

SRM UNIVERSITY DELHI-NCR, SONEPAT (HARYANA)

VISION

SRM University Delhi-NCR, Sonepat, Haryana aims to emerge as a leading world-class university that creates and disseminates knowledge upholding the highest standards of instruction in Medicine & Health Sciences, Engineering & Technology, Management, Law, Science & Humanities. Along with academic excellence and skills, our curriculum imparts integrity and social sensitivity to mould our graduates who may be best suited to serve the nation and the world.

MISSION

1. To create a diverse community campus that inspires freedom and innovation.
2. Promote excellence in educational & skill development processes. Continue to build productive international alliances.
3. Explore optimal development opportunities available to students and faculty.
4. Cultivate an exciting and rigorous research environment.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VISION

Department is committed to provide Intellectual, Innovative & Inspirational environment and contribute to academic, scientific, research and technical knowledge through excellence and to produce technocrats, researchers and bureaucrats.

MISSION

1. To improve the problem-solving capability of students through continual learning to produce quality engineers and researcher in the field of VLSI Design, Microelectronics, Embedded system design and circuit design.
2. To bridge the gap between industry and academia by bringing state-of-the-art technology.
3. To encourage innovation through multidisciplinary research and development activities.
4. To inculcate human values and ethics into students to serve the society in all possible ways

SEMESTER-I

Code	Category	Course	L	T	P	C
Theory						
	OE	Open Elective-I	4	0	0	4
24MIC0101	PC	Semiconductor Devices & Modeling	4	0	0	4
24MIC0103	PC	VLSI-CAD	4	0	0	4
24MIC0105	PC	CMOS Digital VLSI Design	4	0	0	4
	DE	Departmental Elective-I	4	0	0	4
Practical						
24MIC0121	PC	Microelectronics Lab-I	0	0	4	3
Total			**20**	**1**	**4**	**23**
Total Contact Hours			**25**			

SEMESTER-II

Code	Category	Course	L	T	P	C
Theory						
24MIC0102	PC	Analog VLSI Design	4	1	0	4
24MIC0104	PC	VLSI Process Technology	4	0	0	4
24MIC0106	PC	FPGA and Reconfigurable System	4	0	0	4
	DE	Department Elective-II	4	0	0	4
	DE	Department Elective-III	4	0	0	4
Practical						
24MIC0122	PC	Microelectronics Lab-II	0	0	4	3
Total			**20**	**1**	**4**	**23**
Total Contact Hours			**25**			

SEMESTER-III

Code	Category	Course	L	T	P	C
Theory						
24MIC0201	PC	Mixed Signal system Design	4	1	0	4
	DE	Department Elective-IV	4	0	0	4
Practical						
24MIC0251	PC	Seminar	0	0	0	4
24MIC0271	PC	Dissertation Phase-I	0	0	16	8
Total			**12**	**1**	**16**	**20**
Total Contact Hours			**29**			

SEMESTER-IV

Code	Category	Course	L	T	P	C
Practical						
24MIC0272	PC	Dissertation Phase-II	0	0	24	12
Total			**0**	**0**	**24**	**12**
Total Contact Hours			**24**			

Total Credits: 78

LIST OF OPEN AND DEPARTMENTAL ELECTIVES

Code	Category	Course	L	T	P	C
Open Elective						
24MOE0101	OE	Research Methodology	4	0	0	4
24MOE0103	OE	Advance Mathematics and Computations	4	0	0	4
24MOE0105	OE	Nano Technology	4	0	0	4
24MOE0107	OE	Engineering Economics and Management	4	0	0	4
24MOE0109	OE	Industrial Management	4	0	0	4
24MOE0011	OE	Reliability and quality Management	4	0	0	4
24MOE0015	OE	Entrepreneurship Development	4	0	0	4
Departmental Elective-I						
24MIE0101	DE	Modeling of MOS Devices	4	0	0	4
24MIE0103	DE	VLSI Architecture	4	0	0	4
24MIE0105	DE	Device Physics and Technology	4	0	0	4
Departmental Elective-II						
24MIE0102	DE	Memory Design and Testing	4	0	0	4
24MIE0104	DE	High Speed VLSI Design	4	0	0	4
24MIE0106	DE	Fault Tolerance in VLSI	4	0	0	4
Departmental Elective-III						
24MIE0108	DE	Advanced Analog Circuit Design Techniques	4	0	0	4
24MIE0011	DE	System on Chip Design	4	0	0	4
24MIE0015	DE	Photonics Devices and Circuits	4	0	0	4

Departmental Elective-IV						
24MIE0201	DE	Low Power VLSI Design	4	0	0	4
24MIE0203	DE	VLSI Subsystem Design	4	0	0	4
24MIE0205	DE	Application Specific IC Design (ASIC Design)	4	0	0	4
24MIE0207	DE	MEMS Design	4	0	0	4
24MIE0209	DE	Nano-electronics	4	0	0	4
24MIE0211	DE	Artificial Intelligence & Neural Network	4	0	0	4

		L	T	P	C
24MIC0101	**SEMICONDUCTOR DEVICE AND MODELING**	**4**	**0**	**0**	**4**
	Prerequisite				
	Nil				

COURSE OBJECTIVES

1. In this course the students will learn fundamental of semiconductor physics, quantum mechanics, carrier transport, MOSFET modelling and its analysis.

OUTCOME

2. Understand the basic theory of MOS transistors.
3. Acquire knowledge about physics involved in modelling of semiconductor device.
4. 2. Acquire the basic knowledge about quantum mechanical fundamentals.
5. 3. Model MOSFET devices.

UNIT	CONTENTS	HOURS
UNIT-I:	Basic Phenomenon: Energy bands in Si, Carrier transport in Si, Basic equation for device operation. P-N junction: Depletion region, V-I Characteristics, Transport behaviour and noise, Terminal Functions. –n junction: Built in potential and Applied Potential, Abrupt junction Diffusion capacitance. Introduction to BJT.	9
UNIT-II:	Heterojunction, Metal-Semiconductor contacts, Formation of barrier, current transport process, Measurement of barrier Height , Ohmic Contacts.	9
UNIT-III:	MOS Capacitor: Surface and Electrostatic potential, charge distribution, capacitance in MOS, Polysilicon work function and depletion effects, MOS under Non equilibrium and gate diodes, Si- SiO2 interface, Effects of Oxide and interface trapped charges. High Field Effects: Impact Ionization and avalanche breakdown, Band to band Tunneling into and trough SiO2, Injection of hot carriers, High Field effects in Gated Diodes, Dielectric breakdown. FET family tree, versions of FET, Introduction to JEFTs, MESFETs and MOSFETs.	9
UNIT-IV:	Long Channel MOSFETs: Drain current model, I-V characteristics, sub threshold characteristics, Substrate bias and temperature dependence of VT, Channel mobility, capacitance effect. Short Channel MOSFETs: Short channel effect, Velocity saturation, channel length modulation, Source Drain series resistance, MOSFET breakdown. CMOS Device Design: MOSFET scaling, threshold voltage, channel Length. CMOS performance factor: Basic CMOS circuit elements, Parasitic elements, sensitivity of CMOS delay to device parameters.	9
UNIT-V:	Ebers-Moll, Gummel-Poon model for BJT. Outline of numerical Approach to 2D and 3D device models. Introduction to PSPICE and ATLAS tools for device simulation. Simple examples of device modelling and Simulation. Futuristic semiconductor devices, Optoelectronic devices.	9

TEXT BOOKS

1. Sze, S.M., Physics of Semiconductor Devices, John Wiley and Sons (2008) 2nded.
2. Millman, J. and Halkias, C., Integrated Electronics, Tata McGraw Hill (1972).

REFERENCE BOOKS

3. Muller, R.S. and Kamins, T.I., Device Electronics for Integrated Circuits, Wiley (2007) 3rded.
4. Richman P., MOS Field Effect Transistor and Integrated Circuits, John Wiley (1973).

		L	T	P	C
24MIC0103	**VLSI-CAD**	**4**	**0**	**0**	**4**
	Prerequisite				
	Nil				

COURSE OBJECTIVES

In this course the students will learn logic synthesis with design optimization techniques, VHDL design concepts, Combinational logic concepts, sequential VHDL processing and FPGA.

OUTCOME

1. Model digital systems in VHDL at different levels of abstraction.
2. Partition a digital system into different subsystems.
3. Simulate and verify a design.
4. Transfer a design from a version possible to simulate to a version possible to synthesize.

UNIT	CONTENTS	HOURS
UNIT-I:	VHDL: Behavioral, Data Flow and Structural modeling, Data objects and Data types, Basic system (combinational and sequential) design examples using different modeling styles.	9
UNIT-II:	VHDL Statements Control, and case statements, loops, generics, subprograms, attributes, FSM design using VHDL.	9
UNIT-III:	CAD FOR VLSI: Hierarchical view of VLSI design; Architectural design; High level synthesis.	9
UNIT-IV:	CAD FOR VLSI Scheduling; data path synthesis, minimization technique.	9
UNIT-V:	CAD FOR VLSI: Circuit design and simulation; layout synthesis; placement and routing; DRC; Silicon compiler.	9

TEXT BOOKS

1. Naylor, D. and Jones, S., VHDL: A Logic Synthesis Approach, Springer (1997).
2. Bhaskar, J., A VHDL Primer, Pearson Education/ Prentice Hall (2006)3rd Ed.
3. Rushton, A., VHDL for Logic Synthesis, Wiley (1998) 2nd Ed.

REFERENCE BOOKS

4. Ashenden, P., The Designer's Guide to VHDL, Elsevier (2008) 3rd Ed.

		L	T	P	C
24MIC0105	**CMOS DIGITAL VLSI DESIGN**	**4**	**0**	**0**	**4**
	Prerequisite				
	Nil				

COURSE OBJECTIVES

To understand the physics and modeling of MOSFETs, basic theory of fabrication steps and layout of CMOS Integrated Circuits, basic theory of Power Dissipation in CMOS Digital Circuits and Foster ability to work with static and dynamic logic circuits.

OUTCOME

1. Understand the basic Physics and Modeling of MOSFETs.
2. Learn the basics of Fabrication and Layout of CMOS Integrated Circuits.
3. Study and analyze the performance of CMOS Inverter circuits on the basis of their operation and working.
4. Study the Static CMOS Logic Elements.
5. Study the Dynamic Logic Circuit Concepts and CMOS Dynamic Logic Families.

UNIT	CONTENTS	HOURS
UNIT-I:	Device Physics: Review of MOS Transistor Theory, MOS Device Equations, Basic DC Equations, Concept of Threshold voltage, Second Order Effects, Small Signal ac Characteristics.	9
UNIT-II:	Inverter Analysis: Complementary CMOS Inverter DC Characteristics, βn/βp Ratio, Noise Margin, CMOS Inverter as an Amplifier, Static Load CMOS Inverters ,Pseudo NMOS Inverter, Saturated Load Inverters, Cascode Inverter, TTL Interface Inverter, Differential Inverter, Transmission Gate, Tri-state Inverter, BiCMOS Inverters, Stick Diagrams Design Rules, Layout Design , Latch- up in CMOS.	9
UNIT-III:	Circuit Characterization and Performance Estimation: Resistances and Capacitances Estimation, SPICE Modeling, Switching Characteristics, Delay Models, Rise and Fall times, Propagation Delays, Body Effect, CMOS Gate Transistor Sizing, Power Dissipation, Design Margining, Scaling Principles.	9
UNIT-IV:	CMOS Circuit and Logic Design: CMOS Logic Gate Design, Basic Physical Design of Simple Logic Gates, CMOS Logic Structures, Clocking Strategies.	9
UNIT-V:	VLSI Design Methodologies: VLSI Design Flow, Structured Design Strategies, VLSI Design Styles, Chip Design Options.	9

TEXT BOOKS

1. Kang, S. and Leblebici, Y., CMOS Digital Integrated Circuits – Analysis and Design, Tata McGraw Hill (2008) 3rd ed.
2. Weste, N.H.E. and Eshraghian, K., CMOS VLSI Design: A Circuits and Systems Perspective, Addision Wesley (1998) 2nd ed.
3. Rabaey, J.M., Chandrakasen, A.P. and Nikolic, B., Digital Integrated Circuits – A Design Perspective, Pearson Education (2007) 2nd ed.

REFERENCE BOOKS

1. Paker, R.J., Lee, H. W. and Boyce, D. E., CMOS Circuit Design, Layout and Simulation, Wiley - IEEE Press (2004) 2nd ed.
2. Weste, N.H.E., Harris, D. and Banerjee, A., CMOS VLSI Design, Dorling Kindersley (2006) 3rd ed.

		L	T	P	C
24MIC0121	**MICROELECTRONICS LAB-I**	**0**	**0**	**4**	**3**
	Prerequisite				
	Nil				

COURSE OBJECTIVES

To provide the handout on the CAD tools for VLSI system design.

OUTCOME

1. The candidate will be able to design and simulate the system.
2. The candidate will be able to analyse the given system with specifications.

Students will have to complete ANY FIVE experiments from the following list during the first semester.

List of Experiments:

1. Study of Resistive Load NMOS inverter and its simulation for VI characteristics using Mentor Graphics tool (Design Architect)
2. Study of COMS inverter and its simulation for VI characteristics using Mentor Graphics tool (Design Architect).
3. Study of COMS inverter and its simulation for VI characteristics using Mentor Graphics tool (Design Architect) at different W/L ratios.
4. Study of Differential Amplifier and its simulation for VI characteristics using Mentor Graphics tool (Design Architect)
5. Verification of behavior of Half adder using VHDL and its synthesis/implementation on Xilinx ISE.
6. Verification of behavior of half adder using VHDL and its synthesis/implementation on Xilinx ISE.
7. Verification of behavior of S-R Latch using VHDL and its synthesis/implementation on Xilinx ISE.
8. Verification of behavior of D Flip-Flop using VHDL and its synthesis/implementation on Xilinx ISE.

REFERENCE BOOKS

Laboratory Reference Manual.

		L	T	P	C
24MIC0102	**ANALOG VLSI DESIGN**	**4**	**1**	**0**	**4**
	Prerequisite				
	19MIC0105				

COURSE OBJECTIVES

1. To introduce analog MOS processes layout techniques, single stage amplifiers, working of differential amplifiers with frequency response, and noise impact.

OUTCOME

1. Apply knowledge of mathematics, science, and engineering to design and analysis of analog integrated circuits.
2. Identify, formulates, and solves engineering problems in the area of analog integrated circuits.
3. Use the techniques, skills, and modern programming tools such as Mentor Graphics, necessary for engineering practice.
4. Participate and function within multi-disciplinary teams.

UNIT	CONTENTS	HOURS
UNIT-I:	Basic MOS Device Physics: MOS IV Characteristics, second order effects, short-channel effects, MOS Device Models, Review of small signal MOS Transistor Models, MOSFET Noise. Analog MOS Process: Analog CMOS Process (Double Poly Process), Digital CMOS Process tailored to analog IC fabrication, Fabrication of active Devices , Passive Devices and interconnects, analog layout techniques.	9
UNIT-II:	Single Stage Amplifier: Common source Stage, Source Follower, Common Gate Stage, Cascode, Folded Cascode. Differential Amplifier: Single Ended and Differential Operation, Qualitative and Quantitative Analysis, Current Sources and Mirrors: Current sources, basic current mirrors, cascade current mirrors. Frequency Response of Amplifiers: Miller Effect, Association of Poles with Notes, Frequency Response of All Single Stage amplifiers	9
UNIT-III:	Voltage References: Different Configurations of Voltage References, Major Issues, Supply Independent Biasing, Temperature-Independent References. Feedback: General Considerations, Topologies, Effect of loading. Operational Amplifier: General Considerations Theory and Design, Performance Parameters, Single –stage Op Amps, Two - stage Op Amps.	9
UNIT-IV:	Stability and Frequency Compensation: General Considerations, Multi-Pole systems Phase Margin, Frequency Compensation, Compensation techniques. Noise: Noise Spectrum, Sources, Types, Thermal and flicker noise, Representation in circuits, Noise Bandwidth, Noise Figure. Switched-Capacitor Circuits:	9
UNIT-V:	Non Linearity and Mismatch: Nonlinearity of Differential Circuits, Effect of Negative Feedback, Capacitor Nonlinearity, Linearization Techniques, Offset Cancellation Techniques, Reduction of Noise by Offset Cancellation.	9

TEXT BOOKS

1. Razavi, B., Design of Analog CMOS Integrated Circuits, Tata McGraw Hill (2008).
2. Gregorian, R. and Temes, G.C., Analog MOS Integrated Circuits for Signal Processing, John Wiley (2004).
3. Allen, P.E. and Holberg, D.R., CMOS Analog Circuit Design, Oxford University Press (2002) 2nd ed.

REFERENCE BOOKS

4. Johns, D.A. and Martin, K., Analog Integrated Circuit Design, John Wiley (2008).

5. Gray, P.R., Hurst, P.J., Lewis, S.H., and Meyer, R.G., Analysis and Design of Analog Integrated Circuits, John Wiley (2001) 5th ed.

		L	T	P	C
24MIC0104	**VLSI PROCESS TECHNOLOGY**	**4**	**0**	**0**	**4**
	Prerequisite				
	19MIC0101				

COURSE OBJECTIVES

To understand basic theory of Crystal Growth and Wafer Preparation, Epitaxy, Diffusion and Ion-implantation, Oxidation, Lithography, Etching and Nano-Fabrication.

OUTCOME

1. Understand the basic steps of fabrication.
2. Learn the basics theory of Crystal Growth and Wafer Preparation.
3. Study the Epitaxy, Diffusion, Oxidation, Lithography and Etching.
4. Understand the basic theory of Nano-Fabrication.

UNIT	CONTENTS	HOURS
UNIT-I:	Crystal Growth and Oxidation: Starting material, The Czochralski Technique, Silicon Float – Zone process, Material characterization. Thermal Oxidation process, Impurity redistribution, Masking properties of SiO2, Oxide quality, oxide thickness characterization.	9
UNIT-II:	Photolithography and Etching: Clean room, masks, photoresists, Optical lithography, resolution enhancement techniques, and next generation lithography methods. Wet etching: Si etching, SiO2 etching, Si3N4 etching, Polysilicon etching, Al etching and GaAs etching. Dry Etching: Plasma fundamentals, Reactive ion etching techniques and applications.	9
UNIT-III:	Diffusion and Ion Implantation: Diffusion equation, diffusion profile, extrinsic diffusion, laterals diffusion. Ion distribution, ion stopping, Implant damage and annealing.	9
UNIT-IV:	Film Deposition: Epitaxial growth techniques, Dielectric deposition, Polysilicon deposition, Metallization.	9
UNIT-V:	Process Integration: Passive components, MOSFET Technology Bipolar Technology, MEMS Technology.	9

TEXT BOOKS

1. VLSI Technology by S.M. Sze, Tata McGraw Hill.
2. Silicon VLSI Technology: Fundamentals, Practice and Modeling – by Jam es D Plummer, Deal & Griffin; PHI.

REFERENCE BOOKS

1. Yannis Tsividis, Mixed Analog-Digital VLSI Device and Technology, World Scientific, 2002.

		L	T	P	C
24MIC0122	**MICROELECTRONICS LAB-II**	**0**	**0**	**4**	**3**
	Prerequisite				
	Nil				

COURSE OBJECTIVES

The objective of this laboratory is to provide the handout to the students on the SPICE tool and the implement any function FPGA hardware.

OUTCOME

2. Students will be able to understand and simulate the design specification sing SPICE tools.
3. Able to design and analyse the given circuit.
4. GPGA implementation will enable them to practically analyse the given specification.

Students will have to complete experiments from the following list during the second semester.

List of Experiments:

1. Study of Layout of NMOS inverter and its simulation for VI characteristics using Mentor Graphics tool (IC Station).
2. Study of Layout of COMS inverter and its simulation for VI characteristics using Mentor Graphics tool (IC Station).
3. Study of Layout of COMS inverter and its simulation for VI characteristics using Mentor Graphics tool (IC Station) at different W/L ratios.
4. Study of Layout of Transmission Gate and its simulation for VI characteristics using Mentor Graphics tool (IC Station).
5. FPGA implementation of Half adder using Xilinx ISE and Spartan 3A/Vertex II Pro. kit.
6. FPGA implementation of Full adder using Xilinx ISE and Spartan 3A/Vertex II Pro kit.
7. FPGA implementation S-R Latch using Xilinx ISE and Spartan 3A/Vertex II Pro kit.
8. FPGA implementation of D Flip-Flop using Xilinx ISE and Spartan 3A/Vertex II Pro kit.

REFERENCE BOOKS

Laboratory Reference Manual.

		L	T	P	C
24MIC0201	**MIXED SIGNAL SYSTEM DESIGN**	**4**	**0**	**0**	**4**
	Prerequisite				
	19MIC0102				

COURSE OBJECTIVES

In this course the students will learn basics of comparator circuits, data converters, implementation converters and their performance analysis with design challenges.

OUTCOME

1. Apply knowledge of mathematics, science, and engineering to design CMOS analog circuits to achieve performance specifications.
2. Identify, formulates, and solves engineering problems in the area of mixed-signal design.
3. Use the techniques and skills for design and analysis of CMOS based switched capacitor circuits.
4. Work as a team to design, implement, and document a mixed-signal integrated circuit

UNIT	CONTENTS	HOURS
UNIT-I:	Introduction: Device Models, IC Process for Mixed Signal, Concepts of MOS Theory. Comparators: Circuit Modeling, Auto Zeroing Comparators, Differential Comparators, Regenerative Comparators, Fully Differential Comparators, Latched Comparator. Data Converters: Requirements, Static and Dynamic Performance, SNR and BER, DNL, INL.	9
UNIT-II:	High Speed A/D Converter Architectures: Flash, Folding, Interpolating, pipelined High Speed D/A Converter Architectures: Nyquist-Rate D/A Converters, Thermometer Coded D/A Converters, Binary Weighted D/A Converters. Design of multi-channel low level and high level data acquisition systems using ADC/DAC, SHA and Analog multiplexers, Designing of low power circuits for transducers.	9
UNIT-III:	Sigma-Delta Data Converter Architectures: Programmable Capacitor Arrays (PCA), Switched Capacitor converters, Noise Spectrum, Sigma-Delta Modulation Method, Sigma-Delta A/D and D/A Converters, Non Idealities. Key Analog Circuit Design: Analog VLSI building blocks, Operational Amplifiers for converters, advanced op-amp design techniques, Voltage Comparators, Sample-and-Hold Circuits.	9
UNIT-IV:	Implementation and Design of High Performance A/D and D/A Converters: System Design, Digital Compensation, Noise, and Mismatch, Layout and Simulation Technologies for Data Converters. Design Challenges: Low Voltage Design, Ultra-High Speed Design, High Accuracy Design.	9
UNIT-V:	Advanced Topics: Multipliers, Oscillators, Mixers, Passive Filter Design, Active filter design, Switched Capacitor Filters, Frequency Scaling, Phase-Locked Loops, Device Modeling for AMS IC Design, Concept of AMS Modeling and Simulation.	9

TEXT BOOKS

1. Baker, R.J., Li, H.W. and Boyce, D.E., CMOS: Circuit Design, Layout and Simulation, IEEE Press (2007) 2nd ed.
2. Gregorian, R. and Temes, G.C., Analog MOS Integrated Circuits for Signal Processing, Wiley (2002).

REFERENCE BOOKS

1. Gregorian, R., Introduction to CMOS Op-Amps and Comparators, Wiley (1999).
2. Jespers, P.G. A., Integrated Converters: D-A and A-D Architectures, Analysis and Simulation, Oxford University Press (2001).

		L	T	P	C
24MIC0251	**SEMINAR**	**0**	**0**	**0**	**4**
	Prerequisite				
	Nil				

COURSE OBJECTIVES

In this course the students will learn basics of research survey and identify the key finding from them.

OUTCOME

1. Student will be able to identify the latest trends and tools in the area of VLSI design.
2. Will be able to understand the key points of the latest research.
3. Will be able to explain the findings of his/he survey to the audience.

		L	T	P	C
19MIC0271	**DISSERTATION PHASE-I**	**0**	**0**	**16**	**8**
	Prerequisite				
	Nil				

COURSE OBJECTIVES

In this course the students will learn how to implement the given design specification and analyse the same design specification.

OUTCOME

1. Will be solely able to implement any design specification on the provided tool and platform.
2. Will come up with a design that will be fully functional and may be implemented on the hardware platform.

		L	T	P	C
24MIC0272	**DISSERTATION PHASE-II**	**0**	**0**	**24**	**12**
	Prerequisite				
	Nil				

COURSE OBJECTIVES

1. To identify a small research problem, do the survey for that, implement the design and finally produce a detailed report on that.

OUTCOME

1. Will be able to understand the research work of any other researcher.
2. Will be able to identify a research problem.
3. Will be able to do the literature survey on the identified research problem.
4. Will be solely able to implement the problem and able to analyse the results.
5. Will be able to write a thesis report on the aforesaid implementation and analysis.

DEPARTMENT ELECTIVES

		L	T	P	C
24MIE0101	**MODELING OF MOS DEVICES**	**4**	**0**	**0**	**4**
	Prerequisite				
	Nil				

COURSE OBJECTIVES

In this course the students will learn fundamental of semiconductor physics, quantum mechanics, carrier transport, MOSFET modelling and its analysis.

OUTCOME

1. Acquire knowledge about physics involved in modelling of semiconductor device.
2. Acquire the basic knowledge about quantum mechanical fundamentals.
3. Model MOSFET devices.
4. Identify characteristics of Advanced Device Technology

UNIT	CONTENTS	HOURS
UNIT-I:	**Semiconductor Fundamentals:** Poisson and Continuity Equations, Recombination, Equilibrium carrier concentrations (electron statistics, density of states, effective mass, band gap narrowing, Review of PN and MS diodes. **Quantum Mechanics Fundamentals:** Basic Quantum Mechanics, Crystal symmetry and band structure, 2D/1D density of states, Tunneling.	9
UNIT-II:	**Modeling and Simulation of Carrier Transport:** Carrier Scattering (impurity, phonon, carrier-carrier, remote/interface), Boltzmann Transport Equation, Drift-diffusion. **MOS Capacitors:** Modes of operation (accumulation, depletion, strong/weak inversion), Capacitance versus voltage, Gated diode, Non-ideal effects (poly depletion, surface charges), High field effects (tunneling, breakdown).	9
UNIT-III:	**MOSFET Modeling:** Introduction Interior Layer, MOS Transistor Current, Threshold Voltage, Temperature Short Channel and Narrow Width Effect, Models for Enhancement, Depletion Type MOSFET, CMOS Models in SPICE, Long Channel MOSFET Devices, Short Channel MOSFET Devices.	9
UNIT-IV:	**Parameter Measurement:** General Methods, Specific Bipolar Measurement, Depletion Capacitance, Series Resistances, Early Effect, Gummel Plots, MOSFET: Long and Short Channel Parameters, Statistical Modeling of Bipolar and MOS Transistors.	9
UNIT-V:	**Advanced Device Technology:** SOI, SiGe, strained Si, Alternative oxide/gate materials, Alternative geometries (raised source/drain, dual gate, vertical, FinFET), Memory Devices (DRAM, Flash). Sub-micron and Deep sub-micron Device Modeling.	9

TEXT BOOKS

1. Tsividis, Y., Operation and Modeling of the MOS Transistor, Oxford University Press, (2008) 2nd ed.
2. Sze, S.M., Physics of Semiconductor Devices, Wiley (2008).
3. Muller, R.S., Kamins, T.I., and Chan, M., Device Electronics for Integrated Circuits, John Wiley (2007) 3rd ed.

REFERENCE BOOKS

1. Taur, Y. and Ning, T.H., Fundamentals of Modern VLSI Devices, Cambridge University Press (2009).
2. Massobrio, G. and Antognetti, P., Semiconductor Device Modeling, McGraw Hill (1998).

		L	T	P	C
24MIE0103	**VLSI ARCHITECTURE**	**4**	**0**	**0**	**4**
	Prerequisite				
	Nil				

COURSE OBJECTIVES

The motive of this course is to inculcate the knowledge of the different processors; their architecture and organizational intricacies. For performance enhancement consideration is given to various instruction level and memory management techniques such as pipeling, parallelism, instruction scheduling, hierarchical memory management etc.

OUTCOME

1. To review the basics of different processors including architecture and organization
2. To foster ability of handling and designing different types of pipelining techniques; exception handling corresponding instruction scheduling.
3. To understand various memory organization and management techniques

UNIT	CONTENTS	HOURS
UNIT-I:	**Introduction:** Review of basic computer architecture, quantitative techniques in computer design, measuring and reporting performance. CISC and RISC processors. Processor organization and Architectural Overview	9
UNIT-II:	**Pipelining:** Basic concepts, instruction and arithmetic pipeline, data hazards, control hazards, and structural hazards, techniques for handling hazards. Exception handling. Pipeline optimization techniques, dynamic instruction scheduling	9
UNIT-III:	**Hierarchical memory technology:** Inclusion, Coherence and locality properties; Cache memory organizations, Techniques for reducing cache misses; Virtual memory organization, mapping and management techniques, memory replacement policies.	9
UNIT-IV:	**Instruction-level parallelism:** basic concepts, techniques for increasing ILP, superscalar, super-pipelined and VLIW processor architectures. Array and vector processors.	9
UNIT-V:	**Multiprocessor architecture:** taxonomy of parallel architectures. Centralized shared-memory architecture: synchronization, memory consistency, interconnection networks. Distributed shared-memory architecture Superscaler Processors: Overview, Design Issues.	9

TEXT BOOKS

1. Hennessy, J.L., Patterson, D.A, and Goldberg, D., Computer Architecture A Quantitative Approach, Pearson Education Asia (2006) 4th ed.
2. Leigh, .E. and Ali, D.L., System Architecture: software and hardware concepts, South Wester Publishing Co. (2000).

REFERENCE BOOKS

1. Stallings, W., Computer Organization and Architecture: Designing for Performance, Prentice Hall (2003) 7th ed.
2. Parhami, B., Computer Arithmetic Algorithms and Hardware Design, Oxford (2000).

		L	T	P	C
24MIE0105	**DEVICE PHYSICS AND TECHNOLOGY**	**4**	**0**	**0**	**4**
	Prerequisite				
	Nil				

COURSE OBJECTIVES

To understand the physics of semiconductor, basic theory of Metal Semiconductor Contacts and PN junction, construction and operation of BJT and MOSFET and basic theory, operation and structure of MOS transistors, basic theory of Crystal Growth and Wafer Preparation, Epitaxy, Diffusion and Ion-implantation, Oxidation, Lithography, Etching and Nano-Fabrication.

OUTCOME

1. Understand the basic physics of semiconductor devices and the basics theory of PN junction.
2. Understand the basic theory of MOS transistors.
3. Understand the basic steps of fabrication.
4. Learn the basics theory of Crystal Growth and Wafer Preparation.
5. Study the Epitaxy, Diffusion, Oxidation, Lithography and Etching.
6. Understand the basic theory of Nano-Fabrication.

UNIT	CONTENTS	HOURS
UNIT-I:	Semiconductor Physics: Semiconductor Materials, Crystal Structure, Energy Bands, Carrier Concentrations, Carrier Transport Phenomena, Continuity Equation, Thermionic Emission Process, Tunneling Process, High Field Effects.	9
UNIT-II:	Semiconductor Devices: p-n Junction, Thermal Equilibrium Condition, Depletion Region and Capacitance, IV and CV characteristics, Charge storage, Transient Behaviour, Junction Breakdown, Metal Semiconductor Contacts, Tunnel diode-applications of tunnelling, Photonic Devices-LEDs	9
UNIT-III:	Semiconductor Laser, Photodiode, Bipolar Transistor - Static Characteristics, Frequency Response and Switching, Thyristor, MOSFET Fundamentals and Scaling, MESFET, CMOS.	9
UNIT-IV:	Semiconductor Technology: Crystal Growth, , Epitaxial- Growth Techniques, Structures and Defects, Film Formation, Deposition methods, Thermal Oxidation, Dielectric Deposition, Polysilicon and High-K dielectric, Lithography, Next Generation Lithographic Methods.	9
UNIT-V:	Dry and Wet Chemical Etching, Impurity Doping, Diffusion-Related Processes, Implant-Related Processes, Annealing, Metallization, Integrated Devices, CMOS Fabrication Process, IC Packaging, Material and Device Characterisation.	9

TEXT BOOKS

1. S. M. Sze, Semiconductor Devices – Physics and Technology, 2nd Edition, Wiley, 2010.
2. Yannis Tsividis, Mixed Analog-Digital VLSI Device and Technology, World Scientific, 2002.

REFERENCE BOOKS

1. Yannis Tsividis, Operation and modeling of the MOS transistor, Mc Graw Hill, 1987.
2. S. M Sze, VLSI Technology, 2nd Edition, Tata Mc Graw Hill, 2003.

		L	T	P	C
24MIE0102	**MEMORY DESIGN AND TESTING**	**4**	**0**	**0**	**4**
	Prerequisite				
	Nil				

COURSE OBJECTIVES

In this course the students will learn overview of memory chip design, DRAM circuits, voltage generators, performance analysis and design issues of ultra-low voltage memory circuits.

OUTCOME

1. Acquire knowledge about Basics of memory chip Design and Technology.
2. Acquire knowledge about RAM and DRAM Design.
3. Know about On-Chip Voltage Generators.
4. Work using Laplace Trans., CTFT and DTFT.
5. Acquire knowledge about High-Performance Subsystem Memories

UNIT	CONTENTS	HOURS
UNIT-I:	Introduction to Memory Chip Design: Basics of Semiconductor Memory, Internal Organization of Memory Chips, Memory Cell Array, Peripheral Circuit, I/O Interface Categories of Memory Chip, History of Memory-Cell Development, Architectures of memory cell: SRAM Cell, DRAM Cell Trends in Non-Volatile Memory Design and Technology, Ferroelectric memory, Basic Operation of Flash Memory Cells, Advances in Flash-Memory Design and Technology.	9
UNIT-II:	DRAM Circuits: High-Density Technology, High-Performance Circuits, Catalog Specifications of the Standard DRAM, Basic Configuration and Operation of the DRAM Chip, Chip Configuration, Address Multiplexing, Fundamental Chip, Multi-divided Data Line and Word Line, Read and Relevant Circuits, Write and Relevant Circuits, Refresh-Relevant Circuits, Redundancy Techniques, On-Chip Testing Circuits, High Signal- to-Noise Ratio DRAM Design and Technology, Trends in High S/N Ratio Design, Data-Line Noise Reduction, Noise Sources.	9
UNIT-III:	On-Chip Voltage Generators: Substrate-Bias Voltage (VBB) Generator, Voltage Up Converter, Voltage Down-Converter, Half-VDD Generator, Examples of Advanced On-Chip Voltage Generators.	9
UNIT-IV:	High-Performance Subsystem Memories: Hierarchical Memory Systems, Memory-Subsystem Technologies, High-Performance Standard DRAMs, Embedded Memories. Low-Power Memory Circuits: Sources and Reduction of Power Dissipation in a RAM Subsystem and Chip, Low-Power DRAM Circuits, Low-Power SRAM Circuits.	9
UNIT-V:	Ultra-Low-Voltage Memory Circuits: Design Issues for Ultra-Low-Voltage RAM Circuits, Reduction of the Subthreshold Current, Stable Memory-Cell Operation, Suppression of, or Compensation for, Design Parameter Variations, Power-Supply Standardization, Ultra-Low Voltage DRAM Circuits, Ultra-Low-Voltage SRAM Circuits, Ultra-Low-Voltage SOI Circuits.	9

TEXT BOOKS/ REFERENCE BOOKS

1. Itoh, K., VLSI Memory Chip Design, Springer (2006).
2. Sharma, A. K., Semiconductor Memories: Technology, Testing and Reliability, Wiley- IEEE press (2002).
3. Adams, R. D., High performance Memory Testing: Design Principles, Fault Modeling and Self-Test, Springer (2002).
4. Sharma, A. K., Advanced Semiconductor Memories: Architecture, Design and Applications, John Wiley (2002).

		L	T	P	C
24MIE0104	**HIGH SPEED VLSI DESIGN**	**4**	**0**	**0**	**4**
	Prerequisite				
	Nil				

COURSE OBJECTIVES

In this course the students will learn the basics of VLSI design for high speed processing, methods for logical efforts, logic styles, latching strategies, interface techniques and related issues. **OUTCOME**

1. Acquire knowledge about High Speed VLSI Circuits Design.
2. Identify the basic Back-End-Of -Line Variability Considerations.
3. Understand the Method of Logical Effort.
4. Understand the Circuit Design Margining and Latching Strategies.
5. Understand the Clocking Styles.

UNIT	CONTENTS	HOURS
UNIT-I:	Introduction of High Speed VLSI Circuits Design: Back-End-Of -Line Variability Considerations: Ideal and non-ideal interconnect issues, Dielectric Thickness and Permittivity The Method of Logical Effort: Delay in a logic gate, Multi-stage logic networks, Choosing the best number of stages.	9
UNIT-II:	Deriving the Method of Logical Effort: Model of a logic, Delay in a logic gate, Minimizing delay along a path, Choosing the length of a path, Using the wrong number of stages, Using the wrong gate size.	9
UNIT-III:	Non-Clocked Logic Styles: Static CMOS, DCVS Logic, Non-Clocked Pass Gate Families. Clocked Logic Styles: Single-Rail Domino Logic Styles, Dual-Rail Domino Structures, Latched Domino Structures, Clocked Pass Gate Logic. Circuit Design Margining: Process Induced Variations, Design Induced Variations, Application Induced Variations, Noise	9
UNIT-IV:	Latching Strategies: Basic Latch Design, Latching single-ended logic, Latching Differential Logic, Race Free Latches for Pre-charged Logic Asynchronous Latch Techniques.	9
UNIT-V:	Interface Techniques: Signalling Standards, Chip-to-Chip Communication Networks, ESD Protection. Clocking Styles: Clock Jitter, Clock Skew, Clock Generation, Clock Distribution, Asynchronous Clocking Techniques.	9

TEXT BOOKS

1. Chung-Kang Cheng, John Lillis, Shen Lin and Norman H. Chang, "Interconnect Analysis and Synthesis" A wiley Interscience Publication (2000).
2. Sung-Mo (Steve) Kang, Yusuf Leblebigi, "CMOS Digital integrated circuits analysis and design", by Tata Mcgraw-Hill, (2007).

REFERENCE BOOKS

1. L. O. Chua, C. A. Desoer, and E. S. Kuh, "Linear and Non-linear circuits", McGraw-Hill, 1987.
2. R. E. Matrick, "Transmission lines for digital and communication networks", IEEE press, 1995.
3. Mauricio Marulanda, "Electronic properties of Carbon Nanotubes", InTech publisher 2011.

		L	T	P	C
24MIE0106	**FAULT TOLERANCE IN VLSI**	**4**	**0**	**0**	**4**
	Prerequisite				
	Nil				

COURSE OBJECTIVES

In this course the students will the basics of fault and error models in VLSI arithmetic, fault tolerance strategies, detection and correction techniques and applications of arithmetic units and systems.

OUTCOME

1. Acquire knowledge about fault tolerance in arithmetic circuits.
2. Learn about Fault diagnosis, Fault tolerance measurement.
3. Acquire knowledge about Fault tolerance strategies.
4. Enhance capabilities about applications of fault tolerant designs in arithmetic units and systems.
5. Acquire knowledge on Software reliability models, and methods.

UNIT	CONTENTS	HOURS
UNIT-I:	Motivation of fault tolerance in arithmetic systems, Fault and error models in VLSI arithmetic units, Reliability and fault tolerance definitions, Reliability and availability modeling. Estimation of the reliability and availability of fault tolerant systems, Fault diagnosis, Fault tolerance measurement.	9
UNIT-II:	Fault tolerance strategies: detection, correction, localization, reconfiguration, Error recovery, Error detecting and correcting codes.	9
UNIT-III:	Detection/correction techniques: modular redundancy, time redundancy (e.g., RESO, RERO, REDWC, RETWV, REXO), data coding (e.g., AN codes, residue codes, GAN codes, RBR codes, Berger codes, residue number systems), algorithm-based techniques, Reconfiguration techniques.	9
UNIT-IV:	Applications to arithmetic units and systems (e.g., convolvers, inner product units, FFT units neural networks), Application levels: unit, processing element, subsystem, system. Cost/benefit analysis Fault-tolerant transaction processing systems; Fault-tolerant Networks; Redundant disks (RAID).	9
UNIT-V:	Software reliability models, Software fault-tolerance methods: N-version programming, recovery blocks, rollback and recovery. Architecture and design of fault – tolerant computer systems using protective redundancy.	9

TEXT BOOKS

1. Pradhan, D.K., Fault Tolerant Computer System Design, Prentice Hall (1996).
2. Johnson, B.W., Design and Analysis of Fault Tolerant Digital Systems, Addison Wesley (1989).

REFERENCE BOOKS

1. Nelson, V.P. and Carroll, B. D., Tutorial: Fault Tolerant Computing, IEEE Computer Society Press (1990
2. Slewiorek, D.P., Swarz, R. S. and Peters A.K., Reliable Computer Systems: Design and Evaluation, A K Peters (1998) 3rd ed.

		L	T	P	C
24MIE0108	**ADVANCED ANALOG CIRCUIT DESIGN TECHNIQUES**	**4**	**0**	**0**	**4**
	Prerequisite				
	Nil				

COURSE OBJECTIVES

In this course the students will learn the basic fundamental of OTA architecture, amplifiers, voltage followers, floating gate circuits along with its applications, switched capacitor techniques and implementations.

OUTCOME

1. Apply knowledge of mathematics, science, and engineering to design and analysis of modern analog integrated circuits.
2. Emphasize the design of practical amplifiers, small systems and their design parameter trade-offs.
3. Understand the relationships between devices, circuits and systems.

UNIT	CONTENTS	HOURS
UNIT-I:	Review of basic Op Amps and OTA Architectures, Conventional Op Amps, OP Amp Limitations, 3 dB time constant computation. Nested and Reversed Gm-C Op Amplifiers. Recent settling time techniques, Enhanced Gm-C Amp for Large capacitive load.	9
UNIT-II:	Line Driver Amplifiers, Band gap and references, Low voltage cells, Low Voltage current source implementation, Flipped voltage follower and applications, Rail-to-rail amplifiers, Fully balanced fully symmetric circuits.	9
UNIT-III:	Bulk-driven circuits, Floating Gate circuits and its applications. LDO Fundamentals, Class D amplifiers, Multipliers: Power, linearity and area trade-offs. P-N Rail to Rail Stages and Low Voltage Cells, Voltage References.	9
UNIT-IV:	Common-Mode Feedback & Feedforward: Theory and Practice, Non-linearity issues and Noise Considerations	9
UNIT-V:	Linearized OTA and Fully-Differential OTA: CMFB control techniques. Negative resistors and capacitors. Low Voltage Switched-Capacitor Techniques, Comparators & Sample and Hold circuits, Negative Capacitor and Resistor Implementations	9

TEXT BOOKS

1. Design of Analog CMOS Integrated Circuits, B. Razavi, Tata McGraw Hill (2008).
2. Low-Voltage Low Power Integrated Circuits, E. Sánchez-Sinencio, A. Andreou, IEEE Press, 1999.
3. Gray, P.R., Hurst, P.J., Lewis, S.H., and Meyer, R.G., Analysis and Design of Analog Integrated Circuits, John Wiley (2001) 5th ed.

REFERENCE BOOKS

1. Design of Analog Integrated Circuits & Systems, K.R. Laker, W.M.C. Sansen, McGraw-Hill, New York, 1994.
2. Analog MOS Integrated Circuits for Signal Processing, R. Gregorian, G. Temes, Wiley, 1986.
3. Selected copies of Journal Papers and notes.

		L	T	P	C
24MIE0011	**SYSTEM ON CHIP DESIGN**	**4**	**0**	**0**	**4**
	Prerequisite				
	Nil				

COURSE OBJECTIVES

In this course the students will learn SOC design processes, ASIC design flow, EDA tools, architecture design and test optimization with system integration issues.

OUTCOME

1. Acquire knowledge about Top-down SoC design flow.
2. Understand the ASIC Design flow and EDA tools.
3. Acquire knowledge about Front-end and back-end chip design.
4. Understand the designing communication Networks.
5. Understand the design space exploration.
6. Understand the design methodologies for SoC
7. Understand the relationships between devices, circuits and systems.

UNIT	CONTENTS	HOURS
UNIT-I:	Overview of SOC Design Process: Introduction, Top-down SoC design flow, Metrics of SoC design, Techniques to improve a specific design metric, ASIC Design flow and EDA tools.	9
UNIT-II:	SOC Architecture Design: Introduction, Front-end chip design, Back-end chip design, Integration platforms and SoC Design, Function Architecture Co-design, Designing Communication Networks,	9
UNIT-III:	System Level Power Estimation and Modeling, Transaction Level Modeling, Design Space Exploration, Software design in SoCs.	9
UNIT-IV:	SOC Design and Test Optimization: Design methodologies for SoC, Noise and signal integrity analysis, System Integration issues for SoC, SoC Test Scheduling and Test Integration, SoC Test Resource partition.	9
UNIT-V:	SoC Design Constrained and Noise Estimation.	9

TEXT BOOKS

1. Wolf, W., Modern VLSI Design: System-on-chip Design, Prentice Hall (2002) 3rd ed.
2. Nekoogar, F. and Nekoogar, F., From ASICs to SOCs: A Practical Approach, Prentice Hall (2003).

REFERENCE BOOKS

1. Uyemura, J.P., Modern VLSI Design – SOC Design, Prentice Hall (2001).
2. Rajsuman, R., System-on-a-chip: Design and Test, Artech House (2000).
3. Asheden, P.J. and Mermet J., System-on-Chip Methodologies and Design Languages, Kluwer Academic (2002)

		L	T	P	C
24MIE0015	**PHOTONICS DEVICES AND CIRCUITS**	**4**	**0**	**0**	**4**
	Prerequisite				
	Nil				

COURSE OBJECTIVES

In this course the students will learn basics of optical fiber communication, optical waveguides, light sources, amplifiers, modulators, detectors, optical MEMS & NEMS and silicon photonics.

OUTCOME

1. Understand the fundamentals, advantages and advances in optical communication and integrated photonic devices and circuits.
2. Introduce optical waveguides, detectors, amplifiers, silicon photonics and MEMS applications in photonics.
3. Design, operate, classify and analyze Semiconductor Lasers, LEDs, modulators and other integrated photonic devices.
4. Identify, formulate and solve engineering-technological problems related optoelectronic integration.

UNIT	CONTENTS	HOURS
UNIT-I:	Introduction to Optical Fiber Communication: Nature of light; optical communication; optical fibers; propagation of light in optical fibers; transmission characteristics of optical fibers; fabrication of optical fibers. Planar Optical Waveguides and Passive Devices: Waveguide classification, step-index waveguides, graded-index waveguides, 3D waveguides, coupled mode theory, grating in waveguide structure, bent waveguides, directional coupler, Bragg reflectors, waveguide filters, AWG, Multiplexer, Demultiplexers.	9
UNIT-II:	Semiconductor Light Sources and Amplifiers: Spontaneous and stimulated emission, emission from semiconductors, semiconductor injection lasers, single frequency lasers, Various laser configurations, injection laser characteristics, VCSEL, LEDs - Introduction, LED power efficiency, LED structures, LED characteristics and Organic LEDs, Optical amplifiers, Semiconductor optical amplifier.)	9
UNIT-III:	Optical Modulators: Electro-optic modulator, Acousto-optic modulator, Electro-absorption modulator, Interferometric modulator, micro-electro-mechanical modulator. Optical Detectors: Optical detection principle, quantum efficiency and responsivity, semiconductor photodiodes with/without internal gain, Solar cell.	9
UNIT-IV:	Optical MEMS and NEMS: Micro-electro-mechanical and nano-electro-mechanical systems, MEMS integrated tunable photonic devices-filters, lasers, hollow waveguides; NEMS tunable devices	9
UNIT-V:	Silicon Photonics: Introduction, Silicon-on-insulator (SOI) Technology, silicon modulators, non-linear silicon photonics, lasers on silicon, CMOS-Photonic hybrid integration, Silicon- germanium detector, Nanophotonics-Photonic crystals, Slow light and its applications.	9

TEXT BOOKS

1. B. E. A. Saleh and M. C. Teich, Fundamentals of Photonics, Wiley (2007).
2. H. Nishihara, M. Haruna, T. Suhara, Optical Integrated Circuits, Mc-Graw Hill (2008).
3. J.M. Senior, Optical Fiber Communications, Pearson Education (2009).
4. G. T. Reed, Silicon Photonics: The state of the art, John Wiley and Sons (2008)

REFERENCE BOOKS

1. H. Ukita, Micromechanical Photonics, Springer (2006).

To understand the causes of the power dissipation in digital ICs, quantitative analysis of power dissipation in VLSI circuits and exploring the low power circuits and architectures for VLSI system.

OUTCOME

1. Understand the need for low power in VLSI.
2. Understand various dissipation types in CMOS.
3. Estimate and analyse the power dissipation in VLSI circuits.

UNIT	CONTENTS	HOURS
UNIT-I:	Introduction: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices. Sources of Power Dissipation: Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.	9
UNIT-II:	Power estimation, Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, Monte Carlo simulation.	9
UNIT-III:	Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy. Low Power Design: Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library, logic level, Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.	9
UNIT-IV:	Leakage Power Minimization Approaches: Variable threshold voltage CMOS (VTCMOS) approach. Multi-threshold-voltage CMOS (MTCMOS), Dual-Vt assignment approach (DTCMOS), Transistor stacking.	9
UNIT-V:	Low Power Static RAM Architecture: Architecture of SRAM array, Reduced Voltage Swings on Bit Lines, Reducing power in memory peripheral circuits	9

TEXT BOOKS

1. Gary K. Yeap, “Practical Low Power Digital VLSI Design”, KAP, 2002
2. Kaushik Roy, Sharat Prasad, “Low-Power CMOS VLSI Circuit Design” Wiley,

REFERENCE BOOKS

1. Rabaey, Pedram, “Low power design methodologies” Kluwer Academic, 1997
2. Anantha Chandrakasan and Robert Brodersen, “Low Power CMOS Design” Standard Pub., 1995

In this course the students will learn data processing elements with various architecture design, PLA design concepts, and memory design with its clock issues.

OUTCOME

1. Acquire knowledge to Design of Data Processing Elements.
2. Design of Control Part of digital logic circuit.
3. Acquire knowledge about Structuring of Logic Design.
4. Identify Clocking Issues in digital system design

UNIT	CONTENTS	HOURS
UNIT-I:	Introduction: Review of Transistor, Inverter Analysis, CMOS Process and Masking Sequence, Layer Properties and Parasitic Estimation. VLSI Design Flow, Design Methodologies, Abstraction Levels. Design of Data Processing Elements: Adder Architectures, Multiplier Architectures, Counter Architectures, ALU Architectures, Design of Storage Elements: Latches, Flip-Flops, Registers, Register Files.	9
UNIT-II:	Design of Control Part: Moore and Mealy Machines, PLA Based Implementation, Random Logic Implementation, Micro- programmed Implementation.	9
UNIT-III:	Structuring of Logic Design: PLA Design, PLA Architectures, Gates Array Cell Design, Concept of Standard Cell Based Design, Cell Library Design.	9
UNIT-IV:	Memory Design: SRAM cell, Various DRAM cells, RAM Architectures, Address Decoding, Read/Write Circuitry, Sense Amplifier and their Design, ROM Design.	9
UNIT-V:	Clocking Issues: Clocking Strategies, Clock Skew, Clock Distribution and Routing, Clock Buffering, Clock Domains, Gated Clock, Clock Tree. Synchronization Failure and Meta-stability.	9

TEXT BOOKS

1. Weste, N.H.E. and Eshragian, K., Principles of CMOS VLSI Design – A Systems Prespective, Addison Wesley (1994) 3rd ed.
2. Rabaey, J.M., Chandrakasan, A., and Nikolic, B., Digital Integrated Circuits - A
3. Design Perspective, Pearson Education (2008) 3rd ed.
4. Wolf, W., Modern VLSI Design, Prentice Hall (2008) 3rd ed.

REFERENCE BOOKS

1. Mead, C. and Conway, L., Introduction to VLSI Systems, B.S. Publisher (1980) 2nd ed.
2. Uyemura, J.P., Circuit design for CMOS VLSI, Springer (2005) 2nd ed.

		L	T	P	C
24MIE0205	**APPLICATION SPECIFIC IC DESIGN (ASIC DESIGN)**	**4**	**0**	**0**	**4**
	Prerequisite				
	Nil				

COURSE OBJECTIVES

The purpose of this course is to introduce the students the basics of designing and using ASIC's. The operation of tools used in the design is also explained.

OUTCOME

1. To give basic knowledge of ASIC internals.
2. To impart knowledge on ASIC types and tools used in the design.
3. To give advance understanding of tools used.

UNIT	CONTENTS	HOURS
UNIT-I:	**INTRODUCTION TO ASICs** Introduction to ASICs – CMOS logic – ASIC library design.	9
UNIT-II:	**PROGRAMMABLE ASICs** Programmable ASICs - Logic cells – I/O cells – Interconnects – Low level design entry: Schematic entry.	9
UNIT-III:	**SIMULATION AND SYNTHESIS** Logic synthesis: A comparator MUX, Inside a logic synthesizer, VHDL and logic synthesis, FSM synthesis, memory synthesis - Simulation: Types of simulation – logic systems – working of logic simulation.	9
UNIT-IV:	**ASIC TESTING** Boundary scan test – Faults – Fault simulation – Automatic test pattern generation – Built in self-test.	9
UNIT-V:	**ASIC CONSTURCTION** System partitioning – Power dissipation – Partitioning methods – Floor planning and placement: Floor planning, placement – Routing: Global routing, detailed routing, special routing.	9

TEXT BOOKS:

1. Smith .M.J.S, "*Application Specific Integrated Circuits*", Addison Wesley Longman Inc. 1996. (Pearson Education Reprint 2006).
2. M. Sarafzadeh. Wong C.K, "*An Introduction to VLSI Physical Design*", McGraw Hill International Edition, 1995.

REFERENCE BOOKS

1. Wolf Wayne, "FPGA Based System Design", Pearson Education, 2005.
2. Design manuals of Altera, Xilinx and Actel.
3. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, "Digital Integrated Circuits", Second Edition

		L	T	P	C
24MIE0207	**MICRO-ELECTRO MECHANICAL SYSTEM (MEMS)**	**4**	**0**	**0**	**4**
	Prerequisite				
	Nil				

COURSE OBJECTIVES

1. Introduction to MEMS and micro fabrication
2. To study the essential material properties
3. To study various sensing and transduction technique
4. To know various fabrication and machining process of MEMS
5. To know about the polymer and optical MEMS

OUTCOME

This course is offered to students to gain basic knowledge on MEMS (Micro electro Mechanical System) and various fabrication techniques. This enables them to design, analyse, fabricate and test the MEMS based components.

UNIT	CONTENTS	HOURS
UNIT-I	**INTRODUCTION TO MEMS AND MICROFABRICATION** History of MEMS Development, Characteristics of MEMS-Miniaturization – Micro-electronics integration - Mass fabrication with precision. Micro fabrication - microelectronics fabrication process- Silicon based MEMS processes- New material and fabrication processing- Points of consideration for processing.	9
UNIT-II	**ELECTRICAL AND MECHANICAL PROPERTIES OF MEMS MATERIALS** Conductivity of semiconductors, crystal plane and orientation, stress and strain – definition – Relationship between tensile stress and strain- mechanical properties of Silicon and thin films, Flexural beam bending analysis under single loading condition- Types of beam- deflection of beam- longitudinal strain under pure bending- Spring constant, torsional deflection, intrinsic stress, resonance and quality factor.	9
UNIT-III	**SENSING AND ACTUATION** Electrostatic sensing and actuation-Parallel plate capacitor – Application-Inertial, pressure and tactile sensor-parallel plate actuator- comb drive. Thermal sensing and Actuations-Thermal sensors-Actuators- Applications-Inertial, flow and infrared sensors. Piezo resistive sensors- piezo resistive sensor material-stress in flexural cantilever and membrane- Application-Inertial, pressure, flow and tactile sensor. Piezoelectric sensing and actuation- piezoelectric material properties- quartz-PZT-PVDF–ZnO- Application-Inertial, Acoustic, tactile, flow-surface elastic waves Magnetic actuation- Micro magnetic actuation principle-Deposition of magnetic materials-Design and fabrication of magnetic coil.	9
UNIT-IV	**BULK AND SURFACE MICROMACHINING** Anisotropic wet etching, Dry etching of silicon, Deep reactive ion etching (DRIE), Isotropic wet etching, Basic surface micromachining process-structural and sacrificial material, stiction and antistiction methods, Foundry process.	9
UNIT-V	**POLYMER AND OPTICAL MEMS** Polymers in MEMS- polymide-SU-8 Liquid crystal polymer (LCP)-PDMS-PMMA-Parylene- Flurocorbon, Application-Acceleration, pressure, flow and tactile sensors. Optical MEMS-passive MEMS optical components-lenses-mirrors-Actuation for active optical MEMS.	9

TEXT BOOKS

1. Chang Liu, "Foundations of MEMS", Pearson International Edition, 2006.

REFERENCE BOOKS

1. Gaberiel M. Rebiz, "RF MEMS Theory, Design and Technology", John Wiley & Sons,2003
2. Charles P. Poole, Frank J. Owens, "Introduction to Nanotechnology" John Wiley & Sons, 2003.

		L	T	P	C
24MIE0209	**NANOELECTRONICS**	**4**	**0**	**0**	**4**
	Prerequisite				
	Nil				

COURSE OBJECTIVES

In this course the students will learn overview of Nanoelectronics and nano devices, its mechanics and technologies, nano fabrication and characterization and its future aspects.

OUT7C.OME

1. Acquire knowledge about Nanoelectronics and shrink down approach.
2. Understand concept behind nano-MOSFET and nano devices.
3. Set up and solve the Schrodinger equation for different types of potentials in one dimension as well as in 2 or 3 dimensions for specific cases.
4. Understand the nanofabrication and characterization facilities

UNIT	CONTENTS	HOURS
UNIT-I	Shrink-down approaches: Introduction to Nanoscale Systems, Length energy and time scales, Top down approach to Nanolithography, CMOS Scaling, Limits to Scaling, System Integration Limits - Interconnect issues, etc. Overview of Nanoelectronics and Devices: The Nano-scale MOSFET, FinFETs, Vertical MOSFETs, Resonant Tunneling Transistors, Single Electron Transistors, New Storage devices, Optoelectronic and Spin electronics Devices.	9
UNIT-II	Basics of Quantum Mechanics: History of Quantum Mechanics, Schrödinger Equation, Quantum confinement of electrons in semiconductor nano structures, 2D confinement (Quantum Wells), Density of States, Ballistic Electron Transport, Coulomb Blockade, NEGF Formalism, Scattering.	9
UNIT-III	Leakage in Nanometer CMOS Technologies: Taxonomy of Leakage: Introduction, Sources, Impact and Solutions. Leakage dependence on Input Vector: Introduction, Stack Effect, Leakage reduction using Natural Stacks, Leakage reduction using Forced Stacks. Power Gating and Dynamic Voltage Scaling: Introduction, Power Gating, Dynamic Voltage Scaling, Power Gating methodologies.	9
UNIT-IV	Nano-Fabrication and Characterization: Fabrication: Photolithography, Electron-beam Lithography, Advanced Nano-Lithography, Thin-Film Technology, MBE, CVD, PECVD Characterization: Scanning Probe Microscopy, Electron Microscopy (TEM, SEM), Photon Spectroscopy, Nano Manipulators.	9
UNIT-V	Future Aspects of Nanoelectronics: Molecular Electronics: Molecular Semiconductors and Metals, Electronic conduction in molecules, Molecular Logic Gates, Quantum point contacts, Quantum dots and Bottom up approach, Carbon Nano-tube and its applications, Quantum Computation and DNA Computation. Overview of Organic Electronics: OLEDs, OLETs, Organic Solar Cells.	9

TEXT BOOKS

1. Lundstorm, M. and Guo, J., Nanoscale Transistors – Device Physics, Modeling and Simulation, Springer (2006).
2. Bhushan, B., Handbook of Nanotechnology, Springer (2007) 2nd ed.
3. Beenaker, C.W.J., and Houten, V., Quantum Transport in Semiconductor Nanostructures in Solid State Physics, Ehernreich and Turnbell, Academic Press (1991).

REFERENCE BOOKS

1. Ferry, D., Transport in Nanostructures, Cambridge University Press (2008).
2. Mitin, V.V. and Kochelap, V.A., Introduction to Nanoelectronics: Science, Nanotechnology, Engineering and Application, Cambridge Press (2008).

		L	T	P	C
24MIE0211	**ARTIFICIAL INTELLIGENCE & NEURAL NETWORK**	**4**	**0**	**0**	**4**
	Prerequisite				
	Nil				

COURSE OBJECTIVES

1. To have an appreciation for and understanding of both the achievements of AI and the theory underlying those achievements.
2. To have an appreciation for the engineering issues underlying the design of AI systems.
3. To have a basic proficiency in a traditional AI language including an ability to write simple to intermediate programs and an ability to understand code written in that language.

OUTCOME

1. Give Understand different types of AI agents
2. Know various AI search algorithms (uninformed, informed, heuristic, constraint satisfaction, genetic algorithms)

UNIT	CONTENTS	HOURS
UNIT-I	Introduction: AI problems, foundation of AI and history of AI intelligent agents: Agents and Environments, the concept of rationality, the nature of environments, structure of agents, problem solving agents, problem formulation. Searching: Searching for solutions, uniformed search strategies – Breadth first search, depth first Search. Search with partial information (Heuristic search) Greedy best first search, A* search Game Playing: Adversial search, Games, minimax, algorithm, optimal decisions in multiplayer games, Alpha-Beta pruning, Evaluation functions, cutting of search.	9
UNIT-II	Knowledge Representation & Reasons logical Agents, Knowledge – Based Agents, the Wumpus world, logic, propositional logic, Resolution patterns in propos ional logic, Resolution, Forward & Backward. Chaining. First order logic. Inference in first order logic, propositional Vs. first order inference, unification & lifts forward chaining, Backward chaining, Resolution.	9
UNIT-III	Characteristics of Neural Networks, Historical Development of Neural Networks Principles, Artificial Neural Networks: Terminology, Models of Neuron, Topology, Basic Learning Laws, Pattern Recognition Problem, Basic Functional Units, Pattern Recognition Tasks by the Functional Units.	9
UNIT-IV	Introduction, Analysis of pattern Association Networks, Analysis of Pattern Classification Networks, Analysis of pattern storage Networks. Analysis of Pattern Mapping Networks. Feedback Neural Networks, Introduction, Analysis of Linear Auto associative FF Networks, Analysis of Pattern Storage Networks.	9
UNIT-V	Future Aspects of Nanoelectronics: Molecular Electronics: Molecular Competitive Learning Neural Networks & Complex pattern Recognition Introduction, Analysis of Pattern Clustering Networks, Analysis of Feature Mapping Networks, and Associative Memory.	9

TEXT BOOKS

1. Artificial Intelligence – A Modern Approach. Second Edition, Stuart Russel, Peter Norvig, PHI/ Pearson Education.
2. Neural Networks Simon Haykin PHI
3. Artificial Neural Networks B. Yagna Narayana, PHI

REFERENCE BOOKS

1. Artificial Intelligence, 2nd Edition, E. Rich and K. Knight (TMH).
2. Artificial Intelligence and Expert Systems – Patterson PHI.
3. Expert Systems: Principles and Programming- Fourth Edn, Giarrantana/ Riley, Thomson.

OPEN ELECTIVES

		L	T	P	C
24MOE0101	**RESEARCH METHODOLOGY**	**4**	**0**	**0**	**4**
	Prerequisite				
	Nil				

COURSE OBJECTIVES

The primary objective of this course is to develop a research orientation among the scholars and to acquaint them with fundamentals of research methods. Specifically, the course aims at introducing them to the basic concepts used in research and to scientific social research methods and their approach. It includes discussions on sampling techniques, research designs and techniques of analysis.

OUTCOME

1. understand some basic concepts of research and its methodologies
2. identify appropriate research topics
3. select and define appropriate research problem and parameters
4. prepare a project proposal (to undertake a project)
5. organize and conduct research (advanced project) in a more appropriate manner
6. write a research report and thesis

UNIT	CONTENTS	HOURS
UNIT-I:	**Introduction to Research** Introduction, Philosophical Underpinnings, Meaning of Research, Objectives of Research, Motivations in Research, Types of Research, Research Approaches, Significance of Research, Scope of Research, Literature Review, Research Methods vs. Research Methodology, Research Process, Research and Scientific Methods, Criteria of Good Research, Research Questions, Research problem, Selecting the Problem, Necessity and Techniques of Research Problem, Qualitative & Quantitative Research, Research Proposal, Synopsis, Transdisciplinarity, Multidisciplinarity and Interdisciplinarity in Research.	9
UNIT-II:	**Data Collection & Sampling** Collection of Primary Data/Sources, Secondary Data/Sources, Observation Method, Interview, Libraries, Archives & Repositories, Questionnaire, Schedules, Case Study and other Innovative Methods, Research Procedure. Sampling, Steps and Criteria for selecting a Sample procedure, Characteristics of Good Sampling, Types of Sample Design, Selecting Random Samples, Complex Random Sampling Design.	9
UNIT - III:	**Data Analysis & Interpretation** Measures of Central Tendency, Dispersion, Correlation & Regression, Chi-Square Test: applications, Steps, Characteristics, Limitations, Analysis of Variance & Co-variance. Hypothesis: Meaning, Basic Concepts, Flow Diagram, Testing, of Means, Testing of Hypothesis testing of Correlation coefficients, Limitations of Tests of Hypothesis Theory & Empirical approaches, Ethnographic, Comparative and Interpretative Research.	9
UNIT - IV:	**Research Tools and Ethics in Research** Computer Fundamentals, Basics, Data Representation, Word Processing Package, Creating & Editing a Word Document. Ethical issues related to Publishing & Plagiarism, LaTex tool for Detection and Elimination of Plagiarism, Intellectual Property Rights, Copy Rights & Patent Laws.	9
UNIT-V:	**Research Report & Presentations** Structure & Components of Research Report, Types of Report, Layout of Research Report, Mechanism of Writing a Research Report. Presentation: Tailoring the presentation to the target audience, Oral Presentation, Poster Presentation, Submission of Research Article, Thesis Writing, Visual & Delivery.	9

TEXT BOOKS

1. Adam Pzreworsky and Frank Solomon. On the Art of Writing Proposals, rev. edn, New York, 1995.
2. Blaxter Loraine, Hughes Christina and Tight Malcolm. How to Research, Open University Press, 2006.
3. Gerard Guthrie. Basic Research Methods, Sage, London, 2010.
4. Kothari, C. R. Research Methodology: Methods and Techniques, New Age Publishers, Delhi, 2018.

REFERENCE BOOKS

1. Rand R. Wilcox, Fundamentals of Modern Statistical Research, Springer, New York, 2010.
2. Ross, Timothy J. Fuzzy Logic with Engineering Applications, 2nd Edn. Wiley Publications, 2005.

		L	T	P	C
24MOE0103	**ADVANCE MATHEMATICS AND COMPUTATIONS**	**4**	**0**	**0**	**4**
	Prerequisite				
	Nil				

COURSE OBJECTIVES

In this course the students will learn advance mathematics involved in the electronics. This course is also intended towards the modeling of the various systems and statistical test.

OUTCOME

1. Acquire knowledge about advance mathematics involved in the electronics engineering.
2. Will be able to model the system and its analysis.
3. Will be able to apply the various test for the statistical analysis.

UNIT	CONTENTS	HOURS
UNIT-I:	Linear, partial and special differential equation, Different coordinate systems and its conversion, Laplace, Fourier and z- transform, Empirical law of the curve fitting, distribution functions (binomial, Poision, normal, uniform, exponential, rectangular) and Tests (T,F,X2).	9
UNIT-II:	Method for numerical solution of algebraic and transcendental equations: Direct methods: Bisection method, Regula-Falsi method; iterative method: Newton-Raphson method, Rate of convergence, Interpolation, Newton forwarded and backward interpolation, Lagrange's and Newton's divided difference for unique interval.	9
UNIT-III:	Numerical differentiation and integration method, Simpsion's rules, Trapezoidal rule and Romberg's method, Numerical solution of ordinary differential equations: Euler method, modified Euler method and Runge-kutta methods	9
UNIT-IV:	Introduction, definition of modeling and simulation, different types of models, Application of mathematical modeling.	9
UNIT-V:	Continuity equation, energy equation, equation of motion, transport equation, equation of states, phase and chemical equilibrium.	9

TEXT BOOKS

1. Tsividis, Y., Operation and Modeling of the MOS Transistor, Oxford University Press, (2008) 2nd ed.
2. Sze, S.M., Physics of Semiconductor Devices, Wiley (2008).
3. Muller, R.S., Kamins, T.I., and Chan, M., Device Electronics for Integrated Circuits, John Wiley (2007) 3rd ed.

REFERENCE BOOKS

1. Taur, Y. and Ning, T.H., Fundamentals of Modern VLSI Devices, Cambridge University Press (2009).
2. Massobrio, G. and Antognetti, P., Semiconductor Device Modeling, McGraw Hill (1998).

		L	T	P	C
24MOE0105	**NANO TECHNOLOGY**	**4**	**0**	**0**	**4**
	Prerequisite				
	Nil				

COURSE OBJECTIVES

The objective of this course is to make students familiar with the important concepts applicable to small electronic devices, their fabrication, characterization and application.

OUTCOME

The students will be exposed to the various opportunities in the emerging field of nano electronics and nano technologies

UNIT	CONTENTS	HOURS
UNIT-I:	**LIMITATIONS OF CMOS** Fundamentals of MOSFET devices - Scaling of CMOS – Limitations – Alternative concepts in materials – **Structures of MOS devices:** SOI MOSFET, FINFETS, Dual Gate MOSFET, Ferro electric FETs.	9
UNIT-II:	**MICRO AND NANO FABRICATION** Optical Lithography – Electron beam Lithography – Atomic Lithography – Molecular beam epitaxy - Nano lithography.	9
UNIT-III:	**CHARACTERIZATION EQUIPMENTS** Principles of Electron Microscopes – Scanning Electron Microscope – Transmission Electron Microscope - Atomic Force Microscope – Scanning Tunneling Microscope	9
UNIT-IV:	**NANO DEVICES – I** Resonant tunneling diodes – Single electron devices – Josephson junction – Single Flux Quantum logic – Molecular electronics.	9
UNIT-V:	**NANO DEVICES – II** **Quantum computing**: principles – Qrbits – Carbon nanotubes (CNT): Characteristics, CNTFET, Application of CNT - Spintronics: Principle, Spin valves, Magnetic Tunnel Junctions, Spin FETs, MRAM.	9

TEXT BOOK

1. Rainer Waser (Ed.), "Nano electronics and information technology", Wiley- VCH, Edition II, 2005.

REFERENCE BOOKS

1. Thomas Heinzel, "A Microscopic Electronics in Solid State Nanostructure" , Wiley- VCH.
2. Mick Wilson, Kamali Kannangara, Geoff Smith, Michelle Simmons and Burkhard Raguse "Nanotechnology – (Basic Science and Emerging Technologies)", Overseas Press.
3. Mark Ratner and Daniel Ratner, "Nanotechnology: A Gentle Introduction to the Next Big Idea", Pearson education, 2003.

		L	T	P	C
24MOE0107	**ENGINEERING ECONOMICS AND MANAGEMENT**	**4**	**0**	**0**	**4**
	Prerequisite				
	Nil				

COURSE OBJECTIVES

1. Understand the various key concepts of micro economics.
2. Demonstrate the effect of time value of money and depreciation.
3. Apply the various project management techniques
4. Understand the various issues related to industrial safety.

OUTCOME

To provide engineering students with the management skills to enable them to assess, evaluate and take key management decisions by the application of management concepts.

UNIT	CONTENTS	HOURS
UNIT-I:	Role and Importance of Economics for Engineers, Law of demand and supply, Break-even analysis, pricing Policies.	9
UNIT-II:	Cost determination, Balance Sheet, Cost benefit analysis, Time Value of Money, Methods of Depreciation, Long Term and short term financing, Financial Institutions.	9
UNIT-III:	Management-Nature and functions, Project Management-Phases and Techniques, CPM, PERT, Human Aspects of Project Management-Issues and Problems, Managing-vs-leading a project.	9
UNIT-IV:	Marketing Concepts, Marketing Mix, Product life cycle, Plant layout, and Plant location, Material Handling, Productivity, Plant Maintenance and Industrial Safety.	9
UNIT-V:	Current Trends in financing, Role of Industrial Engineer and Applications of Industrial Engineering, Process of Project Management and the Future, Ethics and Project Management, E-Marketing-Ethical and legal issues.	9

TEXT BOOKS

1. R. Pannerselvam, “Engineering Economics”, PHI, 2001.
2. O.P. Khanna, “Industrial Engineering and Management”, Dhanpat Rai and sons, 1992.

REFERENCE BOOKS

1. Kotler, “Marketing Management”, Pearson education, 12th edition.
2. Prasanna Chandra, “Finance Sense for non-finance executives”, TMH.

		L	T	P	C
24MOE0109	**INDUSTRIAL MANAGEMENT**	**4**	**0**	**0**	**4**
	Prerequisite				
	Nil				

COURSE OBJECTIVES

1. To understand the strategic planning, management, entrepreneurship, organisation, production and learning works in an industrial company,
2. To Understand the industrial company markets and price it's products,
3. To understand how the company deal with it's environment.

OUTCOME

1. choose, prepare, interpret and use cost estimates as a basis for the different situations in an industrial company,
2. interpret financial statements and other financial reports of industrial companies, including the income statement, the balance sheet, the cash flow statement and key measures in these,
3. describe how management control of results, action, people and culture functions in an industrial company,

UNIT	CONTENTS	HOURS
UNIT-I:	**Introduction to Management:** Entrepreneurship and organization – Nature and Importance of Management, Functions of Management, Taylor's Scientific Management Theory, Fayol's Principles of Management, Maslow's Theory of Human Needs, Douglas McGregor's Theory X and Theory Y, Herzberg's Two- Factor Theory of Motivation, Systems Approach to Management, Leadership Styles, Social responsibilities of Management	9
UNIT-II:	**Designing Organizational Structures:** Departmentation and Decentralization, Types of Organization structures – Line organization, Line and staff organization, functional organization, Committee organization, matrix organization, Virtual Organization, Cellular Organization, team structure, boundary less organization, inverted pyramid structure, lean and flat organization structure and their merits, demerits and suitability.	9
UNIT-III:	**Operations Management:** Objectives- product design process- Process selection-Types of production system (Job, batch and Mass Production),-Plant location-factors-Urban-Rural sites comparison- Types of Plant Layouts-Design of product layout-Line balancing(RPW method) Value analysis-Definition-types of values- Objectives- Phases of value analysis- Fast diagram	9
UNIT-IV:	**Work Study:** Introduction – definition – objectives – steps in work study – Method study – definition – objectives – steps of method study. Work Measurement –purpose – types of study – stop watch methods – steps – key rating – allowances – standard time calculations – work sampling. Statistical Quality Control: variables-attributes, Shewart control charts for variables- X chart, R chart, – Attributes-Defective-Defect- Charts for attributes-p-chart -c chart (simple Problems), Acceptance Sampling- Single sampling- Double sampling plans-OC curves.	9
UNIT-V:	**Job Evaluation:** methods of job evaluation – simple routing objective systems classification method – factor comparison method – point method – benefits of job evaluation and limitations. Project Management (Pert/Cpm): Network Analysis, Programme Evaluation and Review Technique (PERT), Critical Path Method (CPM), Identifying critical path, Probability of Completing the project within given time, Project Cost Analysis, Project Crashing. (simple problems)	9

TEXT BOOKS

1. Industrial Engineering and Management/O.P. Khanna/Khanna Publishers
2. Industrial Engineering and Management Science/T.R. Banga and S.C. Sarma/Khanna Publishers.

REFERENCE BOOKS

1. Motion and Time Study by Ralph M Barnes/ John Willey & Sons Work Study by ILO
2. Human factors in Engineering & Design/Ernest J McCormick / TMH

		L	T	P	C
24MOE0011	**RELIABILITY AND QUALITY MANAGEMENT**	**4**	**0**	**0**	**4**
	Prerequisite				
	Nil				

COURSE OBJECTIVES

1. To Introduce The Concept Of SQC
2. To Understand Process Control And Acceptance Sampling Procedure And Their Application.
3. To Learn The Concept Of Reliability

OUTCOME

1. Upon Successful Completion Of This Course, The Students Can Able To Apply The Concept Of SQC In Process Control For Reliable Component Production

UNIT	CONTENTS	HOURS
UNIT-I:	**INTRODUCTION AND PROCESS CONTROL FOR VARIABLES** Introduction, Definition Of Quality, Basic Concept Of Quality, Definition Of SQC, Benefits And Limitation Of SQC, Quality Assurance, Quality Control: Quality Cost-Variation In Process Causes Of Variation –Theory Of Control Chart- Uses Of Control Chart – Control Chart For Variables – X Chart, R Chart And □Chart -Process Capability – Process Capability Studies And Simple Problems. Six Sigma Concepts	9
UNIT-II:	**UNIT II : PROCESS CONTROL FOR ATTRIBUTES** Control Chart For Attributes –Control Chart For Non-Conforming– P Chart And Np Chart – Control Chart For Nonconformities– C And U Charts, State Of Control And Process Out Of Control Identification In Charts, Pattern Study	9
UNIT-III:	**UNIT III : ACCEPTANCE SAMPLING** Lot By Lot Sampling – Types – Probability Of Acceptance In Single, Double, Multiple Sampling Techniques – O.C. Curves – Producer's Risk And Consumer's Risk. AQL, LTPD, AOQL Concepts-Standard Sampling Plans For AQL And LTPD- Uses Of Standard Sampling Plans.	9
UNIT-IV:	**LIFE TESTING– RELIABILITY** Life Testing – Objective – Failure Data Analysis, Mean Failure Rate, Mean Time To Failure, Mean Time Between Failure, Hazard Rate – Weibull Model, System Reliability, Series, Parallel And Mixed Configuration – Simple Problems. Maintainability And Availability – Simple Problems. Acceptance Sampling Based On Reliability Test – O.C Curves.	9
UNIT-V:	**QUALITY AND RELIABLITY** Reliability Improvements – Techniques- Use Of Pareto Analysis – Design For Reliability – Redundancy Unit And Standby Redundancy – Optimization In Reliability – Product Design – Product Analysis – Product Development – Product Life Cycles	9

TEXT BOOKS

1. Douglas.C. Montgomery, "Introduction to Statistical Quality Control", 4th Edition, John Wiley 2001.
2. Srinath. L.S., "Reliability Engineering", Affiliated East West Press, 1991.

REFERENCE BOOKS

1. John.S. Oakland. "Statistical Process Control", 5th Edition, Elsevier, 2005
2. Connor, P.D.T.O., "Practical Reliability Engineering", John Wiley, 1993

		L	T	P	C
24MOE0015	**ENTREPRENEURSHIP DEVELOPMENT**	**4**	**0**	**0**	**4**
	Prerequisite				
	Nil				

COURSE OBJECTIVES

To Develop And Strengthen Entrepreneurial Quality And Motivation In Students And To Impart Basic Entrepreneurial Skills And Understanding To Run A Business Efficiently And Effectively.

OUTCOME

Upon Completion Of The Course, Students Will Be Able To Gain Knowledge And Skills Needed To Run A Business Successfully.

UNIT	CONTENTS	HOURS
UNIT-I:	**ENTREPRENEURSHIP** Entrepreneur – Types Of Entrepreneurs – Difference Between Entrepreneur And Entrepreneur Entrepreneurship In Economic Growth, Factors Affecting Entrepreneurial Growth.	9
UNIT-II:	**MOTIVATION** Major Motives Influencing An Entrepreneur – Achievement Motivation Training, Self-Rating, Business Games, Thematic Apperception Test – Stress Management, Entrepreneurship Development Programs – Need, Objectives.	9
UNIT-III:	**BUSINESS** Small Enterprises – Definition, Classification – Characteristics, Ownership Structures – Project Formulation – Steps Involved In Setting Up A Business – Identifying, Selecting A Good Business Opportunity, Market Survey And Research, Techno Economic Feasibility Assessment – Preparation Of Preliminary Project Reports – Project Appraisal – Sources Of Information – Classification Of Needs And Agencies.	9
UNIT-IV:	**FINANCING AND ACCOUNTING** Need – Sources Of Finance, Term Loans, Capital Structure, Financial Institution, Management Of Working Capital, Costing, Break Even Analysis, Taxation – Income Tax, Excise Duty – Sales Tax.	9
UNIT-V:	**SUPPORT TO ENTREPRENEURS** Sickness In Small Business – Concept, Magnitude, Causes And Consequences, Corrective Measures – Business Incubators – Government Policy For Small Scale Enterprises – Growth Strategies In Small Industry – Expansion, Diversification, Joint Venture, Merger And Sub Contracting.	9

TEXT BOOKS

1. Khanka. S.S., "Entrepreneurial Development" S.Chand & Co. Ltd. Ram Nagar, New Delhi, 2013.
2. Donald F Kuratko, "Entrepreneurship – Theory, Process and Practice", 9th Edition, Cengage Learning 2014.

REFERENCE BOOKS

1. Hisrich R D, Peters M P, "Entrepreneurship" 8th Edition, Tata McGraw-Hill, 2013.
2. Mathew J Manimala, "Entrepreneurship Theory At Cross Roads: Paradigms And Praxis"